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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/010,426	11/08/2001	Brad R. Lewis	30014200-1006	6022
58328 7590 10/26/2007 SUN MICROSYSTEMS C/O SONNENSCHN NATH & ROSENTHAL LLP P.O. BOX 061080 WACKER DRIVE STATION, SEARS TOWER CHICAGO, IL 60606-1080			EXAMINER KANG, INSUN	
			ART UNIT 2193	PAPER NUMBER
			MAIL DATE 10/26/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/010,426

Applicant(s)

LEWIS ET AL.

Examiner

Insun Kang

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 August 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 29, 32, 34-36, 38-40, 42-44, 46-48, 50-52 and 54-56 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 29, 32, 34-36, 38-40, 42-44, 46-48, 50-52, and 54-56 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. This action is in response to the amendment filed on 8/6/2007.
2. As per applicant's request, claims 29, 36, 39, 40, 42, 44, 46-48, 50, 51, and 56 have been amended and claims 33, 41, 49, and 53 have been canceled.
3. Claims 29, 32, 34-36, 38-40, 42-44, 46-48, 50-52, and 54-56 are pending in the application.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 29, 32, 34-36, 38-40, 42-44, 46-48, 50-52, and 54-56 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Per claims 29, 36, 44, 51, and 56:

The claims recite, "the optimization command comprises increasing or decreasing a node execution time." The limitation is interpreted as: the optimization command comprises decreasing a node execution time. For increasing a node execution time, it is unclear what this limitation means and how such increasing is performed.

Per claims 32, 34, 35, 38-40, 42, 43, 46-48, 50, 52, 54, and 55, these claims are rejected for dependency on the above rejected parent claims.

Claim Rejections - 35 USC § 103

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6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 29, 32, 34-36, 38, 39, 44, 46, 47, 51, 52, and 54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calder et al. (US Pat. 5,963,972) hereafter Calder, in view of Preiss ("Data Flow on a Queue Machine," 1987), and further in view of Iitsuka (US Patent 5,396,627).

Per claim 29:

Calder discloses:

-generating a graph that represents a flow program comprising code segments distributed between the blocks of memory (i.e. col. 4 lines 29-35), the graph comprising nodes corresponding to selected ones of the blocks and arcs corresponding to dependency relationships between the nodes (i.e. col. 9 lines 35-56; col. 3 lines 55-62); and receiving an optimization command to manipulate the generated graph to improve performance of the flow program (i.e. col. 12 lines 25-53).

Calder does not explicitly teach that the flow graph is a data flow graph. However, Preiss teaches a data flow graph representing data within blocks of memory was known in the pertinent art, at the time applicant's invention was made, to maximize parallelism (i.e. page 7 and 13). It would have been obvious for one having ordinary skill in the art to modify Calder's disclosed system to use a data flow model. The modification would be obvious because one having

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ordinary skill in the art would be motivated to reduce execution time as suggested by Preiss (page 7 and 13).

Calder further discloses: performing the optimization command (i.e. "the performance achieved using edge profiles to guide the optimizations in order to eliminate first-generation cache conflict," col. 12 lines 53-60); and performing performance analysis on the data flow program in accordance with the optimization command (i.e. "full path profiling, and other trace collection techniques in order to collect improved temporal locality information...color mapping method to statically formed flow graphs using static program estimation," col. 12 lines 53-60, 12-17).

Calder discloses generating a graph representing a data flow program comprising nodes representing blocks and arcs representing dependencies between blocks, (column 3, line 46 to column 4, line 8), but Calder and Preiss do not explicitly disclose nodes characterized by a node execution time and the optimization command comprises increasing or decreasing a node execution time. However, Iitsuka discloses that nodes characterized by a node execution time and optimization command increasing or decreasing a node execution time were known in the pertinent art, at the time applicant's invention was made, to optimize execution time (i.e. col. 3 lines 45-56). It would have been obvious for one having ordinary skill in the art to modify the disclosed system of Calder and Preiss to incorporate the teachings of Iitsuka. The modification would be obvious because one having ordinary skill in the art would be motivated to optimize the data flow graph reducing the execution time as suggested by Iitsuka (i.e. col. 3 lines 45-56).

Per claim 32:

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Calder further discloses:

- wherein the nodes are placed in an execution queue for processing, and wherein the optimization command specifies re-ordering the nodes in the execution queue (i.e. col. 1 lines 41-58).

Per claim 34:

Calder further discloses:

- wherein the blocks are assigned data operated on by the data flow program and wherein the optimization command specifies setting revised data for a selected block (i.e. col. 1 lines 41-45; col. 12 lines 53-60).

Per claim 35:

Calder further discloses:

wherein the optimization command specifies a performance comparison between selected nodes (i.e. col. 1 lines 59-66).

In regard to claim 36:

Calder discloses: dividing a memory area into blocks and associating each block with at least a portion of the data and with at least one code segment, generating a graph representation of the flow program, the graph representation comprising nodes associated with the blocks, and arcs associated with dependencies between the blocks, and performing an optimization command to manipulate the graph to improve performance of the flow program (i.e. column 1, lines 41 - 58; column 3, line 56 to column 4, line 8). Calder does not explicitly teach that the

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flow graph is a data flow graph. However, Preiss teaches a data flow graph representing data within blocks of memory was known in the pertinent art, at the time applicant's invention was made, to maximize parallelism (i.e. page 7 and 13). It would have been obvious for one having ordinary skill in the art to modify Calder's disclosed system to use a data flow model. The modification would be obvious because one having ordinary skill in the art would be motivated to reduce execution time as suggested by Preiss (page 7 and 13).

Calder further discloses: performing performance analysis on the data flow program (i.e. "full path profiling, and other trace collection techniques in order to collect improved temporal locality information...color mapping method to statically formed flow graphs using static program estimation," col. 12 lines 53-60, 12-17).

Calder discloses generating a graph representing a data flow program comprising nodes representing blocks and arcs representing dependencies between blocks, (column 3, line 46 to column 4, line 8), but Calder and Preiss do not explicitly disclose nodes characterized by a node execution time and the optimization command comprises increasing or decreasing a node execution time. However, Iitsuka discloses that nodes characterized by a node execution time and optimization command increasing or decreasing a node execution time were known in the pertinent art, at the time applicant's invention was made, to optimize execution time (i.e. col. 3 lines 45-56). It would have been obvious for one having ordinary skill in the art to modify the disclosed system of Calder and Preiss to incorporate the teachings of Iitsuka. The modification would be obvious because one having ordinary skill in the art would be motivated to optimize the data flow graph reducing the execution time as suggested by Iitsuka (i.e. col. 3 lines 45-56).

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Per claim 38, it is another method version of claim 32, respectively, and is rejected for the same reasons set forth in connection with the rejection of claim 32 above.

Per claim 39:

Calder further discloses:

wherein the step of performing performance analysis comprises the step of determining execution time for the data flow program (i.e. col. 3 lines 46-67; col. 4 lines 1-8).

Per claims 44, 46, and 47, they are the computer-readable medium versions of claims 36, 38, and 39, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 36, 38, and 39 above.

Per claims 51, 52, 54, and 55, they are the system versions of claims 29, 32, 34, and 35, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 29, 32, 34, and 35 above.

Per claim 56, it is the system version of claims 29 and 36, respectively, and is rejected for the same reasons set forth in connection with the rejection of claims 29 and 36 above.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

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having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims, 40, 43, 48, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calder et al. (US Pat. 5,963,972) hereafter Calder, in view of Preiss ("Data Flow on a Queue Machine," 1987), further in view of Iitsuka (US Patent 5,396,627, and still further in view of Hamada et al. (US Patent 6,493,863) hereafter Hamada.

In regard to claim 40:

"...wherein the step of performing performance analysis comprises the step of simulating execution of the nodes in the graph. "

Calder discloses generating a graph representing a data flow program comprising nodes representing blocks and arcs representing dependencies between blocks (column 3, line 46 to column 4, line 8), but Calder, Preiss, and Iitsuka do not explicitly disclose nodes characterized by execution times and simulating the data flow program in accordance with the node execution times. However, Hamada discloses application program modules represented in a data flow graph that are simulated and determining the execution timing of each of the modules in a second data flow graph (column 2, lines 19 - 45). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the data graph as taught by Calder, Preiss, and Iitsuka with the simulation and determination of node (module) execution times as taught by Hamada, because the combination allows greater efficiency by optimizing characteristics with using threshold value inherent to the module as taught by Hamada at column 2, lines 40 - 45.

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In regard to claim 43:

Calder discloses generating a graph representing a data flow program comprising nodes representing blocks and arcs representing dependencies between blocks (column 3, line 46 to column 4, line 8), but Calder, Preiss, and Iitsuka do not explicitly disclose modification of at least a portion of the data. However, Hamada discloses application program modules, represented in a data flow graph, that are simulated and data is changed repeatedly to achieve optimal threshold values (column 2, lines 19 - 45). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the graph as taught by Calder, Preiss, and Iitsuka with the simulation and determination of node (module) data values as taught by Hamada, because the combination allows greater efficiency by optimizing characteristics with using threshold value inherent to the module as taught by Hamada at column 2, lines 40 - 45.

Per claims 48 and 50, they are the computer-readable medium versions of claims 40 and 43, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 40 and 43 above.

10. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Calder et al. (US Pat. 5,963,972) hereafter Calder, in view of Preiss ("Data Flow on a Queue Machine," 1987), further in view of Iitsuka (US Patent 5,396,627), and still further in view of Kahn et al. (US Patent 6,662,278) hereafter Kahn.

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In regard to claim 42:

"...wherein the optimization command specifies a memory bandwidth, and wherein the step of performing performance analysis comprises the step of determining execution time for the data flow program in accordance with the memory bandwidth."

Calder discloses generating a graph representing a data flow program comprising nodes representing blocks and arcs representing dependencies between blocks and determining the execution timing of each of the modules (column 3, line 46 to column 4, line 8), but Calder, Preiss, and Iitsuka do not explicitly disclose memory bandwidth specification. However, Kahn discloses a memory bandwidth specification for available memory access (Abstract). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the data graph as taught by Calder, Preiss, and Iitsuka with the simulation and determination of node (module) execution times, because the combination allows greater efficiency by optimizing characteristics with using threshold value, and further modified with the a threshold placed on memory bandwidth as taught by Kahn, because the further modification enhances the code depicted in the data graph of Calder with a threshold of memory accesses per unit of time, as taught by Kahn at column 2, lines 54 - 57, further increasing the efficiency of the optimized code.

Response to Arguments

11. Applicant's arguments with respect to claims 29, 32, 34-36, 38-40, 42-44, 46-48, 50-52, 54-56 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Insun Kang whose telephone number is 571-272-3724. The examiner can normally be reached on M-F 8:30-5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MENG AI AN can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

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may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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